

FIG. 1
related art

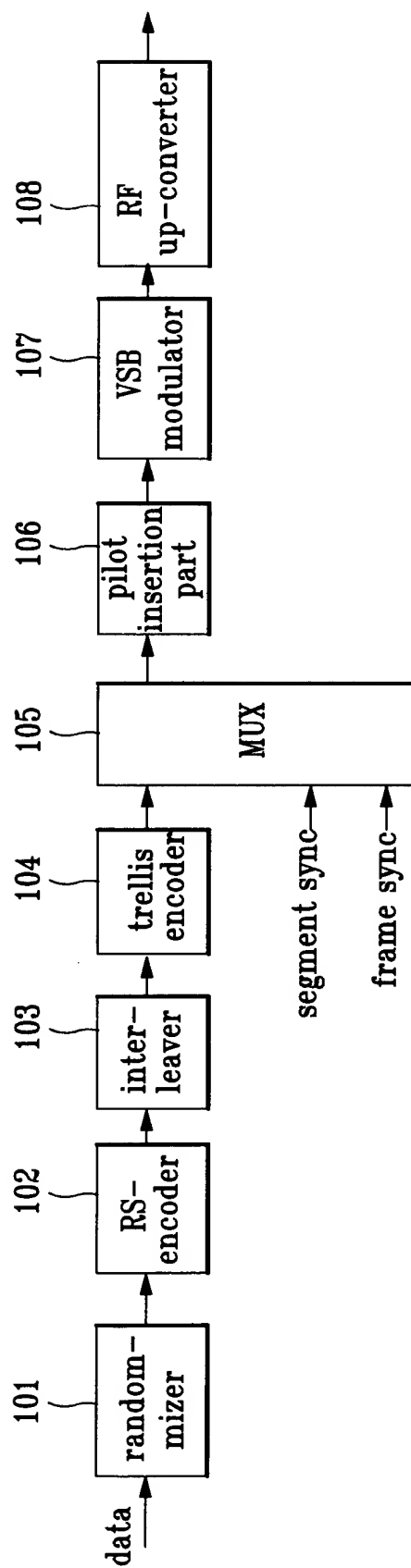


FIG.2a
related art

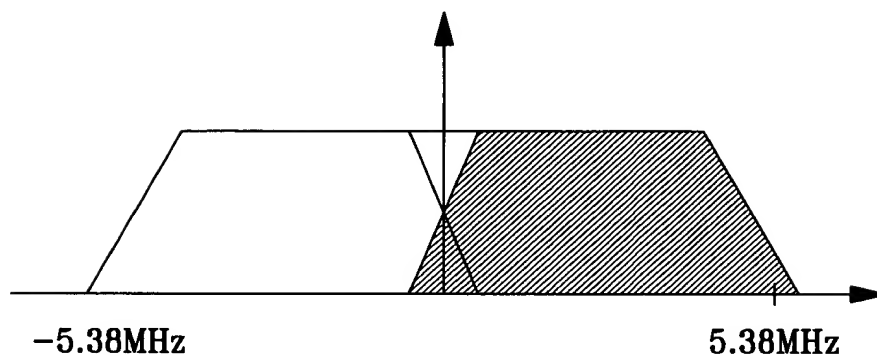
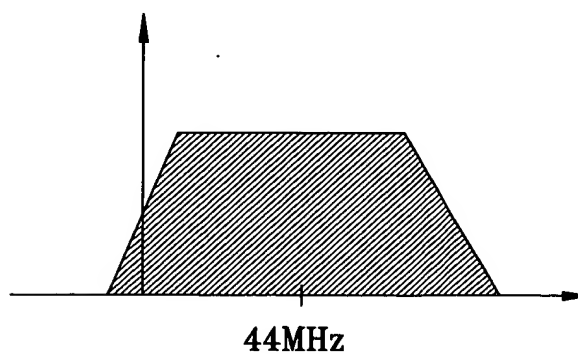
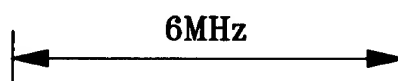
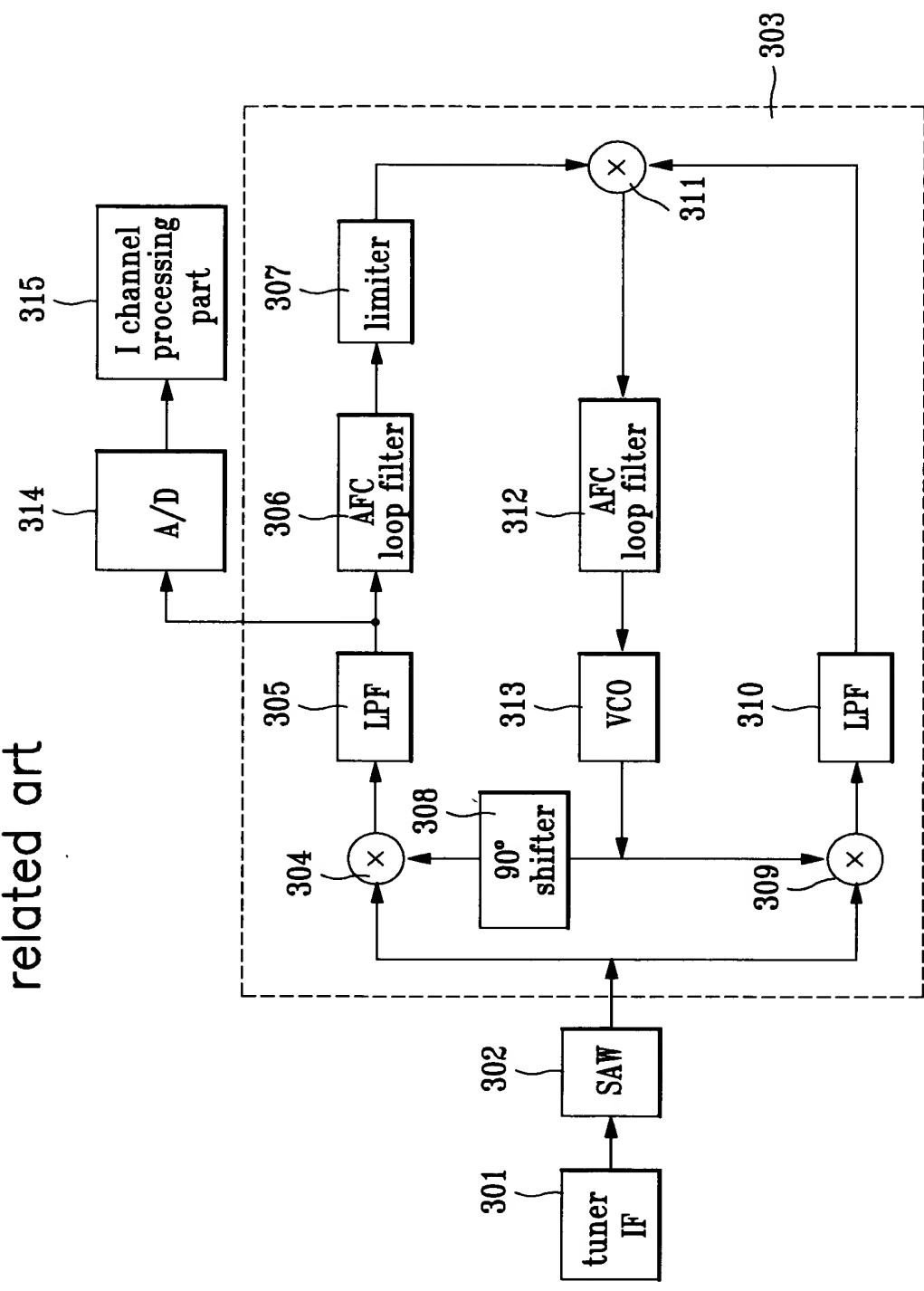


FIG.2b
related art



SECRET CODE 400

FIG.3
related art



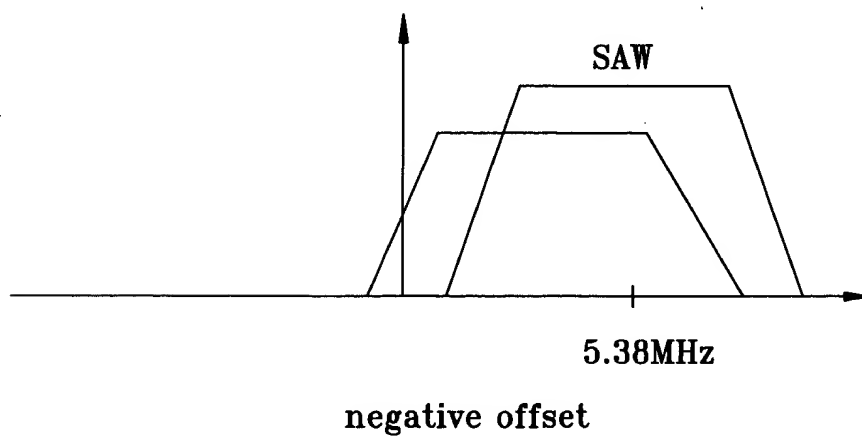
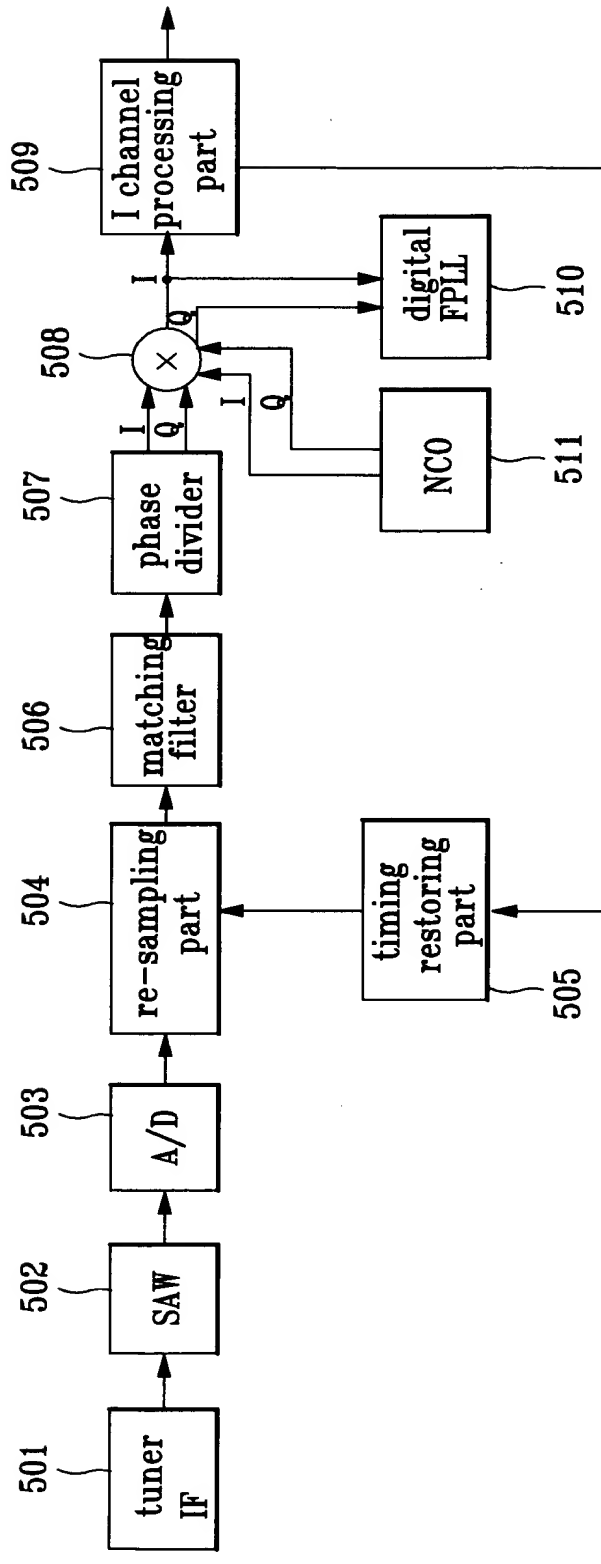
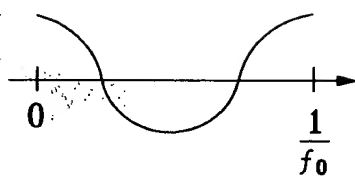


FIG.5
related art

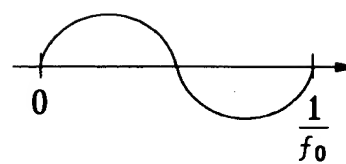


The diagram illustrates a receiver system architecture. The signal path begins with a **tuner IF** block (601), which feeds into a **broad SAW** (Surface Acoustic Wave) filter (602). The output of 602 goes to an **A/D** (Analog-to-Digital) converter (603). The output of 603 is split: one path goes to a **re-sampling part** (604), and the other goes to a **timing restoring part** (605). The output of 604 feeds back into the **A/D** converter (603). The output of 605 feeds back into the **timing restoring part** (605). The output of 605 also feeds into the **I channel processing part** (609). The output of 609 feeds into a **phase divider** (607). The output of 607 feeds into a **matching filter** (606). The output of 606 feeds into a **phase divider** (608). The output of 608 feeds into the **I channel processing part** (609). The output of 609 feeds into the **I channel processing part** (609). The output of 609 feeds into the **I channel processing part** (609).

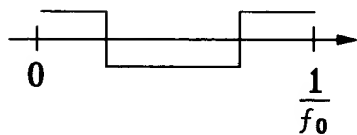
FIG.7



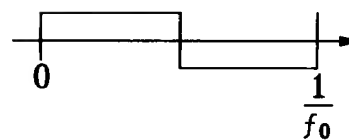
(a)component I



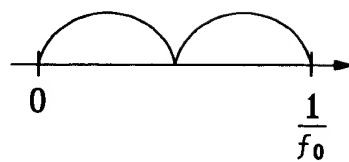
(b)component Q



(c)code value of
component I

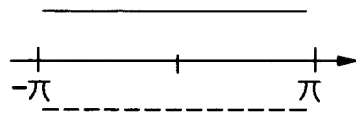


(d)code value of
delayed component I

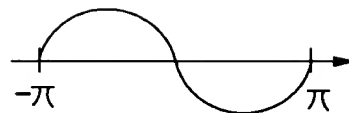


(e)code value of delayed phase
component I * component Q

FIG.8



(a)component I



(b)component Q

FIG.9

